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EXAMINER	
SOUW,B	
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Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary	Application No. 09/116,138	Applicant(s) Anthony et al.
	Examiner Bernard Souw	Group Art Unit 2814

☒ Responsive to communication(s) filed on *Jul 25, 2000*

☒ This action is **FINAL.**

☐ Since this application is in condition for allowance except for formal matters, **prosecution as to the merits is closed** in accordance with the practice under *Ex parte Quayle* 1935 C.D. 11; 453 O.G. 213.

A shortened statutory period for response to this action is set to expire 3 month(s), or thirty days, whichever is longer, from the mailing date of this communication. Failure to respond within the period for response will cause the application to become abandoned. (35 U.S.C. § 133). Extensions of time may be obtained under the provisions of 37 CFR 1.136(a).

Disposition of Claim

☒ Claim(s) *1-30 and 36-45* is/are pending in the applicat

Of the above, claim(s) ______ is/are withdrawn from consideration

☐ Claim(s) ______ is/are allowed.

☒ Claim(s) *1-30 and 36-45* is/are rejected.

☐ Claim(s) ______ is/are objected to.

☐ Claims ______ are subject to restriction or election requirement.

Application Papers

☐ See the attached Notice of Draftsperson's Patent Drawing Review, PTO-948.

☐ The drawing(s) filed on ______ is/are objected to by the Examiner.

☐ The proposed drawing correction, filed on ______ is ☐ approved ☐ disapproved.

☐ The specification is objected to by the Examiner.

☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

☐ All ☐ Some* ☒ None of the CERTIFIED copies of the priority documents have been

☐ received.

☐ received in Application No. (Series Code/Serial Number) ______ .

☐ received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

*Certified copies not received: ______

☒ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

☒ Notice of References Cited, PTO-892

☐ Information Disclosure Statement(s), PTO-1449, Paper No(s). ______

☐ Interview Summary, PTO-413

☐ Notice of Draftsperson's Patent Drawing Review, PTO-948

☐ Notice of Informal Patent Application, PTO-152

— SEE OFFICE ACTION ON THE FOLLOWING PAGES —

DETAILED ACTION

Acknowledgment

1. The Amendment C filed 07/25/2000 under 37 CFR 1.111, Paper No.14, in response to the Office action dated 01/13/2000 has been entered.

No claims has been canceled or amended by the Applicants.

New claims 41-45 have been added.

The present Office action is made with all the suggested amendments being fully considered. Accordingly, pending in this Office action are claims 1-30 and 36-45.

35 U.S.C. 103 (a) Rejections

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 12-23, 26-30, 37, 38 and 40 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hori in view of Hsieh et al.

Hori discloses a method of fabricating a field-effect device on an integrated circuit, comprising the steps of:

- providing a single-crystal silicon substrate 1 shown in Figs.1a-1f, as disclosed in Col.3/line 24.
- forming a high permittivity dielectric layer 3 on the substrate 1, as disclosed in Col.3/ll.28-31.

However, Hori's dielectric layer 3 is made of silicon oxynitride, not metal silicate as recited in the claim. Hsieh et al. use metal silicate 12' as high permittivity dielectric, as shown in Fig.2 and disclosed in Col.4/ll.7-30 & Col.5/ll.19-44, specifically in Col.5/ll.21-22.

Hori as modified by Hsieh continues the process with the step of:

- forming a conductive gate 5 overlying the metal silicate dielectric layer 3, as shown in Fig.1d and disclosed in Col.3/ll.32-34.

It would have been obvious to one having ordinary skill in the art at the time of the invention to fabricate a field effect device using Hori's silicon-oxynitride as high permittivity dielectric layer, thereby adopting Hsieh's metal silicates to replace Hori's silicon-oxynitride, since Hsieh's metal silicates can be formed by a process simpler than Hori's silicon oxynitride, as is generally known in the art (see section Examiner's Response to Applicant's Arguments).

- Regarding claims 12 and 16, the step of depositing a first metal on the silicon substrate in an oxidizing ambient, thereby forming an at least partially oxidized layer on the substrate, is disclosed by Hsieh et al. in Col.6/ll.2-5, whereby silicon dioxide is also formed on the substrate surface, whereas the step of annealing the substrate in an oxidizing

ambient is disclosed in Col.6/ll.5-9. The additional step of claim 16, i.e., depositing silicon in an oxygen ambient, is disclosed by Hsieh in Col.6/ll.2-5.

- Regarding claims 13, 14, 17 and 18, the limitation that the substrate of claim 12 and claim 1 comprises an oxidized silicon surface layer (claim 13) and/or a clean Si surface (claim 14) immediately prior to the depositing step, is an obvious matter of materials design choice within skill in the art.

The limitation of claims 13 and 17, i.e., that the substrate comprises an oxidized silicon surface layer immediately prior to the depositing step, is an obvious matter of process choice within skill in the art, since a silicon surface will be promptly oxidized if left alone in a normal atmosphere.

The limitation of claims 14 and 18 is again an obvious matter of design choice, i.e., whether to use a naturally oxidized surface of silicon, or firstly clean the Si surface before depositing the first metal in an oxidizing ambient to form a partially oxidized metal layer and an oxidized Si surface, as recited in claim 12. It is a general knowledge in the art that the methods of claims 13 and 14 are both applicable to form a metal silicate, as long as the substrate surface is made of silicon. Evidence for such a general knowledge is given by Hsieh et al. in Col.6/ll.2-10., whereby it is obvious that a mixture of metal-oxide and silicon dioxide is produced by sputtering or evaporation in oxygen ambient.

Regarding claims 15 and 20, the step of depositing a first metal by sputtering is disclosed by Hsieh et al. in Col.6/line 4.

- Regarding claim 19, the step of simultaneously, instead of sequentially, depositing a 1st metal and silicon layers of claim 16, both by means of sputtering, is an obvious matter of process choice within skill in the art. Selection of any order of performing process steps is *prima facie* obvious in the absence of new or unexpected results; *In re Burhans*, 154 F.2d 690, 69 USPQ 330 (CCPA 1946).
- Regarding claim 21, the step of simultaneously evaporating the first metal and silicon from a common source is obvious to one ordinary skill in the art, the common source being a metal silicide.
- Regarding claim 22, the step of simultaneously, instead of sequentially, evaporating the first metal and silicon from separate sources is also obvious to one ordinary skill in the art as being a matter of materials choice in regards of claim 21. Furthermore, a metal silicide sputtering source is equivalent to a combination of metal source and a silicon source. Therefore, it would have been obvious to one ordinarily skilled in the art at the time the invention was made to select any one of these sources as a suitable sputtering source, since it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use as a matter of design choice. *In re Leshin*, 125 USPQ 416.
- Regarding claim 23, the step of independently varying the evaporation rate of the separate sources is obvious to one of ordinary skill in the art, since necessary means for such independent variation is conventionally provided by the apparatus. It would have

been desirable to fabricate a metal silicate dielectric layer having a depth-varying ratio of the first metal to silicon, since gate leakage current, gate insulator breakdown, and field-effect carrier mobility can be finely tuned and optimized.

- Regarding claims 26 and 27, the step of exposing a clean Si surface on the substrate is an obvious as also a conventional step as known to one of ordinary skill in the art, as disclosed by Hori in Col.3/line 24. Hsieh et al. deposit a partially reduced metal silicate layer in the form of a metal silicide layer 12 in Fig.1, then anneal (claim 27) the layer 12 in oxygen to form metal silicate layer 12' in Fig.2, as recited in Col.3/ll.3-10.
- Regarding claim 28, the step of simultaneously depositing a metal oxide and silicon by PVD is essentially the same as claim 21 or 22, since evaporation is a PVD method, and also an equivalent alternative of the simultaneous sputtering step recited in claim 20.
- Regarding claims 29 and 30, the step of simultaneously depositing a partially reduced metal silicate layer by means of PVD, whereby the reduced metal silicate layer is a mixture of silicon dioxide with zirconium oxide (claim 29) or hafnium oxide (claim 30), is disclosed by Hsieh et al. in Col.3/ll.34-51. It would have been obvious to one having ordinary skill in the art at the time of the invention to fabricate a field effect device according to Hori's method, thereby adopting Hsieh's method to replace Hori's silicon nitride gate dielectric with metal silicates, since Hsieh's silicate ($ZrSiO_4$) has a higher permittivity ($\epsilon \leq 10.5$) than Hori's silicon oxynitride ($\epsilon \leq 7.5$).

- Claims 37, 38 and 40 are related to claims 12, 24, and 28, respectively, as product by process claims. Claims 37, 38 and 40 are thus rejected by the same paragraphs, reasons and prior arts as applied to their respective parent claims.

3. Claims 2, 3, 24, 25, 36 and 39 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hori in view of Hsieh et al., and further in view of Gardner et al.

Hori as modified by Hsieh et al. show all the limitations of claim 2, as applied previously to claim 1, including the steps of forming metal silicate 18' from a metal silicide layer 18 on a substrate 16, as shown by Hsieh et al. in Fig.5. In particular, Hsieh et al. oxidize the silicide layer 18 to convert into a silicate layer 18' of Fig.6, as recited in Col.5/ll.13-24. However, Hsieh et al. deposit the silicide layer 18 onto a substrate 16 shown in Fig.5 already as metal silicide, instead of forming the silicide layer 18 by a silicidation reaction.

Gardner et al. describe a method of forming various metal silicides for use in a semiconductor device, as disclosed in Col.2/ll.18-23. Gardner's method comprises steps that render obvious all the remaining limitations of claim 2. In particular, Gardner et al.

- expose a clean Si surface as an obvious step in semiconductor device fabrication known to one ordinarily skilled in the art.
- deposit a first metal layer 26 on the Si surface, as shown in Fig.3, followed by the step of annealing in an inert ambient to form a layer of silicide of the first metal layer 26, as

shown by the silicide layer 26/28 in Fig.5A, disclosed by Gardner et al. in Col.6/ll.6-10 & 20-23, and in Col.6/ll.27-38.

Hsieh et al. continue the steps further, using Gardner's reacted silicide layer 26/28 in place of Hsieh's deposited silicide layer 18 in Fig.5.

- The step of oxidizing Gardner's silicide layer 26/28 in place of Hsieh's layer 18 to form a metal silicate layer 18' is disclosed by Hsieh et al. in Col.5/ll.19-66.

It would have been obvious to one having ordinary skill in the art at the time of the invention to modify Hori's method of using high permittivity dielectric as gate dielectric in a field effect device by Hsieh's method of using metal silicates, thereby forming the metal silicide in a silicidation reaction of the silicon substrate and a deposited metal layer as taught by Gardner et al., since the latter is a conventional method for making silicide layers well-known in the semiconductor manufacturing technology.

One would have been motivated to use Gardner's to modify Hori's and Hsieh's, since the use of a standard & conventional method of forming metal silicide as taught by Gardner's would save time and effort in undue experimentations, thus minimizing the overall cost of the device production, while being much less complicated and less messy than depositing by, e.g., CVD.

- Regarding claim 3, the step of oxidizing less than 1 nm clean Si surface prior to depositing the first metal layer is inherent to conventional silicidation reaction process, whereby a natural/native oxide layer of about 5 nm is usually formed prior to the deposition

of the siliciding metal, as disclosed by Gardner et al. in Col.2/ll.24-33. Generally, differences in concentration, temperature, or layer thickness will not support the patentability of subject matter encompassed by the prior art unless there is evidence indicating such concentration or temperature is critical. "Where the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation". *In re Aller*, 220 F.2d 454, 456, 105 USPQ 233, 235 (CCPA 1955).

- Regarding claim 24, the (repeated) step(s) of evaporating an intermediate layer of material onto the substrate, the material selected from the group consisting of silicon, a first metal, and combinations thereof, is disclosed by Gardner et al., whereby a silicide layer is consequently formed during a subsequent annealing step.

- The limitation that the intermediate layer being less than 1 nm thick, is disclosed by Hsieh et al. in Col.3/ll.1-3. Since silicon is consumed during the silicidation reaction, Hsieh's original Ta layer must be (much) less than 4 nm thick. A *prima facie* case of obviousness exists where the claimed ranges and prior art ranges do not overlap but are close enough that one ordinarily skilled in the art would have expected them to have the same properties. *In re* Titanium Metals Corporation of America v. Banner, 778 F.2d 775, 227 USPQ 773 (Fed. Cir. 1985).

- The step of annealing the substrate in an oxidizing ambient, thereby at least partially oxidizing the intermediate layer, is disclosed by Hsieh et al. in Col.5/ll.47-59

• The repeated steps of evaporating the intermediate layer, whether the same layers or in alternating fashion, is a duplication of parts. The court held that mere duplication of parts has no patentable significance unless a new and unexpected result is produced. *In re Harza*, 274 F.2d 669, 124 USPQ 378 (CCPA 1960).

• Regarding claim 25, the step of depositing a first set and a second set of one or more intermediate layers of silicon and the first metal, respectively, in alternating fashion, is a duplication of parts fabricated according to claim 24. The court held that mere duplication of parts has no patentable significance unless a new and unexpected result is produced. In re Harza, 274 F.2d 669, 124 USPQ 378 (CCPA 1960).

• Claims 36 and 39 are related to claims 2 and 24, respectively, as product by process claims. Claims 36 and 39 are thus rejected by the same paragraphs, reasons and prior arts as applied to their respective parent claims.

4. Claims 4-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hori in view of Hsieh et al. and Gardner et al., and further in view of Leas et al.

Hori as modified by Hsieh et al. and Gardner et al. show all the limitations of claims 4-11, as applied previously to claim 2 above, except the specific claim limitations to be addressed individually as follows:

- Regarding claims 4 and 7, the process of forming metal silicate by oxidizing a metal silicide using both an oxidizing gas and a reducing gas is disclosed by Leas in Col.3/ll.46-63.
- Regarding claim 5, the limitation that the oxidizing gas is selected from the group consisting of O_2, H_2O, N_2O, CO_2, and combinations thereof, is disclosed by Hsieh et al. (O_2) in Col.3/ll.3-10 and by Leas (H_2O) in Col.3/ll.53-54.
- Regarding claim 6, the limitation that the reducing gas is selected from the group consisting of CO, H_2, CH_3, and combinations thereof, is inherent to Leas' (over a production of H_2O from CO & H_2) as implicated by the reaction described in Col.3/ll.53-54.
- Regarding claim 8, the step of forming metal silicate layer 12' by exposing the metal silicide 12 of Fig.1 to an oxygen plasma is disclosed by Hsieh et al. in Col.3/ll.1-10.
- Regarding claim 9, the limitation that the oxygen plasma is exposed to ultraviolet radiation is not patentable for being an inevitable result of natural law, since the plasma itself generates an intense ultraviolet radiation, as is well-known to one of ordinary skill in the art. Natural laws, and everything resulting therefrom without any specific and active manipulation done by an inventor, are basically unpatentable. MPEP Chapter 2105 says, "the laws of nature, physical phenomena and abstract ideas" are not patentable subject matter. MPEP Chapter 2105 further determines that only a nonnaturally occurring manufacture or composition of matter is patentable.

Regarding claim 10, the step of annealing th- metal silicate layer in a non-oxidizing environment, thereby densifying the silicate layer, is a conventional step taken after every

deposition or reaction process, and is obvious as also well-known to one of ordinary skill in the art. It would have been obvious to one having ordinary skill in the art at the time of the invention to densify Hsieh's high permittivity gate dielectric after it is formed, since compact, densified material would be less prone to environmental impacts (e.g., oxygen penetration).

- Regarding claim 11, the limitation that the annealing step is carried out at a temperature sufficient to crystallize the silicate layer, is an obvious matter of design choice within skill in the art. It would have been obvious to crystallize the silicate layer, in order to increase both mechanical strength and surface smoothness.

5. New claims 41-45 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hori in view of Hsieh et al.

Hori as modified by Hsieh et al. show all the limitations of new claims 41-45, as applied previously to their respective parent claims 1, 2, 16, 24, and 28, respectively, including the limitation that the first metal recited in claims 2, 16, 24 is zirconium, and the metal silicate layer of claim 28 is zirconium silicate layer.

The use of zirconium as the first metal in claims 2, 16, 24 is effectively the same as the use of zirconium silicate layer in claim 28. This limitation is rendered obvious by Hsieh et al. in Col.3/ll.37.-38.

Response to Applicant's Arguments

6. Applicant's arguments filed on 08/19/99 have been fully considered but they are not persuasive. The following is Examiner's response to Applicant's arguments.

7. Regarding Applicant's argument that there is no teaching or suggestion in the prior arts to combine Hori's with Hsieh's (and formerly also with Kang's), it is noted that Hori's MOS device, being of 100 µm dimension (Col.3/ll.56-57), is not commensurate with state-of-the-art semiconductor device manufacturing technology, which is in the submicron range. The present submicron device dimension requires a very thin gate dielectric, which leads to increased leakage current if scaling law is applied. Applicant's argument against Examiner's increased leakage when scaling law is applied to reduce Hori's 100 µm to submicron dimensions, is inappropriate, since exactly the same reason has been admitted by Applicant in the disclosure on pg.2/ll.20-25 and on pg.3/ll.1-9, especially in lines 11-13.

It is elementary for one of ordinary skill in the art to derive the scaling law for device capacitance, which is proportional to the dielectric permittivity κ (= ϵ/ϵ_0) and inversely proportional to the capacitor dielectric thickness t, i.e., $C \sim \kappa/t$. Hence, the use of dielectric materials with higher permittivity would allow the capacitor dielectric to be made thicker according to the scaling law $t \sim \kappa$. This, in turn would reduce the leakage current, which is inversely proportional to the resistance R, and hence, inversely proportional to

the specific resistance ρ and also inversely proportional to the dielectric thickness t , i.e., $I_{leak} \sim 1/R \sim 1/\rho \cdot t \sim 1/\rho \cdot \kappa$.

It is generally known in the art that the dielectric permittivity of a silicon oxynitride is between those of silicon dioxide (κ=3.9) and silicon nitride (κ=7), as disclosed by Sadahiro (Constitution/ll.1-11), more typically between 4.0 and 5.3, as disclosed by Ito et al. in Col.8/ll.16-19. This is to be compared to Hsieh's data for Ta- and Hf-silicates, as disclosed in Table 1 Col.4/line 16, reciting the permittivity for Ta and Hf being κ=22 and κ=12, respectively. Thus Hsieh's metal-silicate's dielectric permittivities are respectively 5 and 3 times higher than Hori's silicon oxynitride. To scale for the same value of device capacitance the thickness of the metal-silicate capacitor dielectric can be made 5 and 3 times thicker, respectively.

From Hsieh's data disclosed in Table 1 in Col.4/ll.16-27, one of ordinary skill in the art would be able to estimate the specific resistance of Ta-silicate and Hf-silicate, which is about $\rho = 2.4 \cdot 10^{13}$ $\Omega \cdot$cm and $\rho = 4.3 \cdot 10^{13}$ $\Omega \cdot$cm, respectively. These are smaller than the 1.9-2.0$\cdot 10^{14}$ $\Omega \cdot$cm specific resistance of silicon oxynitride (Peters, Col.8/Table II). Hence, the leakage current ($\sim 1/\rho \cdot \kappa$) in Hsieh's metal-silicates tends to be larger, but only about 1.5-1.9 times than that in Hori's silicon oxynitride. However, the much simpler deposition process of metal-silicates, as taught by Hsieh et al.in Col.1/ll.65-68, renders these materials more desirable than Hori's silicon oxynitride for use as gate dielectric material(s). This motivation now replaces the previous one based on leakage current.

Specifically, Hsieh's metal silicates can be formed by a process simpler than silicon dioxide, as disclosed by Hsieh et al. in Col.1/ll.65-68. On the other side, Hori's silicon oxynitride is conventionally more difficult/complicated to form than silicon dioxide, as generally known in the art. Therefore, Hsieh's metal silicates can be formed by a process much simpler than Hori's silicon oxynitride.

8. Regarding Applicant's argument, that there is no evidence to believe that Hsieh's (or Kang's) capacitor dielectrics would be useful as superior gate dielectrics, it is noted that Applicant is denying his own invention/disclosure, in which the same gate dielectric materials as Hsieh's (and Kang's) are used.

Applicant's further argument that one must take account of several properties (e.g., interface states, electron mobilities, band offsets), it is noted that all those are factors well-known to one of ordinary skill in the art, and hence, must have been taken into account in both Hsieh's and Kang's. Applicant's implicated allegation that Hsieh's and Kang's are not primarily concerned about these matters, since Hsieh's and Kang's invention is directed to "memory capacitor", is improper for at least three reasons. At first, the word "memory" is completely absent in the entire Hsieh's disclosure. Secondly, the word "memory" is also completely absent throughout the entire previous Office Action. Thirdly, Kang's was cited only and solely for the use of titanium silicate as a capacitor dielectric having high dielectric constant, not at all for use in a "memory" device.

Since it is noted that Kang's titanium silicate is not being used in Applicant's "invention", in this Office Action Kang's is no longer used as a prior art reference, thus rendering moot Applicant's arguments against Kang's. With or without Kang's, the Examiner's grounds for rejections remain fully valid.

9. Regarding Applicant's argument that Applicant's "intermediate layer has a thickness less than 1 nm", in comparison to Hsieh's 4-16 nm, it is to be emphasized that Hsieh's invention was made in 1982, i.e., 16 years older than Applicant's disclosure (1998). It would have been obvious to one of ordinary skill in the art that the thickness improvement is solely due to the 16 years time difference, and not at all due to Applicant's "invention".

10. The present Office Action contains grounds for rejections which are exactly the same (i.e., word by word) as applied in the previous Office Action (Paper No.12), except for the withdrawal of Kang's as prior art, which is redundant anyway, and hence, does not prevent this Office Action from being made FINAL.

In the same manner, a minor change in the motivation/suggestion for combining the cited prior art references (Hori's and Hsieh's) regarding claim 1 rejection is not seen as an obstacle for making this office Action FINAL.

Applicant's addition of new claims 41-45 does not prevent the Finality of this Office Action, since the grounds for their rejections are inherent in the previous rejections of their respective parent claims, which readily includes Zr-silicate besides Ta- and Hf-silicates.

11. **THIS ACTION IS MADE FINAL.** Applicants are reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Papers related to this application may be submitted directly to Art Unit 2814 by facsimile transmission. Papers should be faxed to Art Unit 2814 via the Technology Center 2800 fax center located in Crystal Plaza 4, room 4C23. The faxing of such papers must conform with the notice published in the Official Gazette, 1096 OG 30 (15 November 1989).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Bernard E. Souw whose telephone number is (703) 305-1481. The examiner can normally be reached on Monday-Friday from 8:30am to 5:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chaudury, Olik, can be reached on (703) 306-2794. The fax number for the organization where this application or proceeding is assigned is (703) 308-7722 or -7724.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Technology Center receptionist at (703) 308-0956.

BES

Bernard E. Souw

September 14, 2000

Tom Thomas

Tom Thomas
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